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Application Serial No. 10/827,333

Responsive to Office Action dated 22 June 2007

REMARKS/ARGUMENTS

This case has been carefully reviewed and analyzed in view of the Office Action dated 22 June 2007. Responsive to the Office Action, Claims 1-10 have been amended and Claims 11-16 are newly inserted. Upon entry of this Amendment Claims 1-16 will be pending.

In the Office Action, the Examiner objected to the use of the phrase “The present invention describes” in the Abstract. Accordingly, the Abstract has been amended to remove the phrase. The Examiner also noted that the Claims “appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors”. The Examiner listed the informalities objected to and noted that appropriate correction is required. Accordingly, the Claims have been amended to more clearly recite the subject matter which Applicant regards as the invention.

The Examiner rejected Claims 9 and 10 under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. Regarding Claim 9, line 5 recites “a bright voltage”. The Examiner noted that this term is not defined in the specification. Claim 10 recites that the switch “includes a NMOS transistor … the switch is a PMOS transistor … and the switch is a CMOS transistor” (emphasis added). The specification does not explain how a single switch is all of these. For examination purposes the

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Examiner noted that the Claim would be treated as if it recites one of these three types, “CMOS transistor”. This being the case, the Examiner noted that there is no accepted definition of this term, as a CMOS device comprises a number of transistors. Accordingly, Claims 9 and 10 have been amended to more clearly recite the subject matter.

The Examiner rejected Claim 2 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claim 2 recites “a photodiode adapted for both N-sub and P-sub of CMOS process” and noted that this is unclear. Accordingly, Claim 12 has been amended to more clearly recite the subject matter.

Additionally, the Examiner rejected Claims 1, 9 and 10 under 35 U.S.C. § 102(b) as being anticipated by the Bock reference (U.S. Patent Application Publication #2002/0033439).

Further, the Examiner rejected Claims 1, 7 and 8 under 35 U.S.C. § 103(a) as being unpatentable over the Mizuno reference (U.S. Patent Application Publication #2002/0190193) in view of the Ikeda reference (U.S. Patent#6,111,606) and Claim 2 under 35 U.S.C. § 103(a) as being unpatentable over Mizuno in view of Ikeda and further in view of the Wang reference (U.S. Patent#6,518,085) and Claims 3 and 4 under 35 U.S.C. § 103(a) as being unpatentable over Mizuno in view of Ikeda and further in view

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of the Iida reference (U.S. Patent Application Publication #2003/0057372) and the Sakamoto reference (U.S. Patent #4,672,453) and Claims 5 and 6 over Mizuno in view of Ikeda and further in view of Sakamoto.

Before discussing the prior art relied upon by the Examiner, it is believed beneficial to briefly review the structure of the invention of the subject Patent Application, as now claimed. The present invention is directed to an integrated image detection system having low noise for transforming an optical current to a voltage signal and uses an optical detecting element, as well as an integrator circuit in combination with a correlated double sampling circuit and an output circuit.

As shown in one of the embodiments, when the switch signal 238 shorts, the NMOS switch 235 and the output signal V_{SH} of the optical detecting element 200 is coupled to the output signal 220 of the integrator. The voltage values on either side of the capacitor 231 which stores a voltage value ($V_{SH} - V_{REF2}$) has the voltage V_{SH} and V_{REF2} on opposing input/output lines. The output signal 220 of the integrator is maintained at the value V_{SH} and thus, the voltage value on the right side of the capacitor 231 as shown in Fig. 2 is V_{REF2} .

Activating the switch signal 218 then shorts the CMOS switch 215 and the output signal V_{SH} of the optical detecting element becomes V_{SL} and is coupled to the output

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signal 220 of the integrator. The voltage values on the right side of the capacitor 231 (as seen in Fig. 2) results in a value of $(V_{SL} - V_{SH}) + V_{REF2}$.

The output signal 220 of the integrator is then formed to V_{SH} and the voltage value on the right side of the capacitor 231 (shown in Fig.2) is V_{REF2} .

Thus, when the switch signal 218 shorts the switch 215, the voltage value on the right side of the capacitor 231 is $(V_{SL} - V_{SH}) + V_{REF2}$. Variations in the fabrication process will influence the voltage values V_{SH} and V_{SL} . Due to the equation relation $(V_{SL} - V_{SH})$, the influencing of the fabrication process variation and noise signals are substantially reduced.

In setting forth the 35 U.S.C. § 102(b) rejection of Claims 1, 9 and 10, the Examiner compared features of Bock's apparatus with claimed elements of the invention of the subject Patent Application. However, the Bock reference is simply directed to an image sensor system with pixel resets. The Bock reference includes a photodiode 60 which is buffered by a source follower N-channel MOS transistor M2. There is a capacitor C_{IN} and a reset switch which may be implemented as an N-channel MOS transistor controlled by a signal applied to a gate. The capacitance C_{IN} is charged by current from the photodiode 60 and then is reset by turning the transistor M1 on/off. A voltage on the charge detection node 62 is transferred through the source follower transistor M2 to the read-out circuit 52 which enables a row selection switch M3. The

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reset and row enable signals are common to a row of pixels in the array 30 and are further generated by the controller 32.

It is true that the Bock reference relates to sample-and-hold switches which are implemented as N-channel MOS transistors M9, M10. However, the duration operation and function is substantially remote from the subject invention concept.

It is respectfully submitted that the Bock system uses a reset switch to reduce the secondary image lag and non-linearity of the system. However, Bock does not teach an integrator circuit with a switch to control the voltage value of the electronic signal periodically in a reset voltage and in a bright voltage.

Additionally, the Bock reference does not generate an output signal having a voltage value which is the difference between the reset voltage and the bright voltage in order to eliminate noise. Neither of these elements for the purposes and objectives of the Applicant are provided in the Bock reference.

Thus, the Bock reference does not provide for: "...wherein the integrator circuit comprises a switch to control the voltage value of the electronic signal periodically in a reset voltage...", as is necessary to now amended Independent Claim 1.

Further, the Bock reference does not provide for: "...a correlated double sampling circuit...generating an output signal with a voltage value of the difference between the

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reset voltage and the bright voltage periodically following the operation of the switch of the integrator circuit...”.

The Bock reference provides common elements well-known in the art, but does not provide the elements in combination as now recited in amended Independent Claim 1 for the purposes and objectives of the subject system.

The Examiner has rejected Claims 1 and 7-8 under 35 U.S.C. § 103 as being obvious in view of the Mizuno Patent Application Publication #2002/0190193 when taken in combination with the Ikeda Patent #6,111,606. The Mizuno, et al. reference is directed to an optical detector device. The Mizuno reference includes a first switch SW₀₁ and a second switch SW₀₂ in combination with the optical detector parts 80₁ – 80_n and an integrator circuit 10. However, the Mizuno reference does not teach or allude to the “correlated double sampling circuit connecting the integrator circuit for reading the electronic signal output from the integrator circuit and generating an output signal with a voltage value which is the difference between the reset voltage and the bright voltage in a periodic manner following operation of the switch of the integrator circuit, as is necessary to the subject invention system.

Ikeda is apparently cited for showing a signal process for an imaging device where sample-and-hold circuit components output corresponding signals. However, even if the sample-and-hold circuit of Ikeda were combined with the Mizuno, et al. reference, such

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would not result in the circuitry of the subject invention system and would not provide for: "...an integrator circuit converting charge produced by the optical detecting element into an electronic signal, wherein the integrator circuit comprises a switch to control the voltage value of the signal periodically in a reset voltage...", as is now necessary to Independent Claim 1 as amended.

Further, even if combined, the Mizuno, et al. reference and the Ikeda reference do not provide for: "...a correlated double sampling circuit connected to the integrator circuit for reading the electronic signal output from the integrator circuit and generating an output signal with a voltage value of the difference between the reset voltage and the bright voltage periodically following the operation of the switch...", as is necessary to Independent Claim 1 as amended.

The Examiner has rejected Claims 3 and 4 under 35 U.S.C. § 103 as being obvious in view of the Mizuno reference when taken in combination with the Ikeda reference and then in further combination with the Iida Patent Publication #2003/0057372 and the Sakamoto Patent #4,672,453. The Iida reference is directed to a solid state infrared imager and is apparently cited by the Examiner for showing an amplifier with CMOS inverters in Fig. 9. The Sakamoto reference is apparently cited by the Examiner for showing an image sensor with a CMOS switch connected to an amplifier.

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However, neither the Iida reference, nor the Sakamoto reference, even when combined with the Mizuno reference in combination with the Ikeda reference, provide for the integrator circuit converting charge produced by the optical element into an electronic signal where the integrator circuit has a switch to control the voltage value of the electronic signal periodically in a reset voltage defined as a voltage when the switch is in an “on” condition and in a bright voltage defined as a voltage when the switch is in an “off” condition with the reset voltage and the bright voltage having differing values, as is necessary to Independent Claim 1 as has previously been discussed. Still further, even when the Iida and the Sakamoto reference are combined, such do not provide for the correlated double sampling circuit connected to the integrator circuit for reading the electronic signal output from the integrator circuit and generating an output signal with a voltage value of the difference between the reset voltage and the bright voltage periodically following the operation of the switch of the integrator circuit, as has previously been discussed.

The Examiner has rejected Claim 2 under 35 U.S.C. § 103 as being obvious in view of the Mizuno reference when taken in combination with the Ikeda reference, and further in combination with the Wang reference. The Wang reference apparently has been cited for showing a CMOS imager where the optical detecting element is a photodiode adapted for both N-sub and P-sub of a CMOS process. The Wang reference

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does not cure the defects of the Mizuno reference and the Ikeda reference, since even if the Wang reference were placed in combination with the Mizuno reference and the Ikeda reference, there is no showing of the "...integrator switch to control the voltage value of the electronic signal periodically in a reset voltage...", as necessary to Independent Claim 1, nor does it show the "...integrator circuit for reading...output from the integrator circuit and generating an output signal with a voltage value of the difference...", as previously discussed.

Claims 5 and 6 have been rejected under 35 U.S.C. § 103 as being obvious in view of Mizuno when taken in combination with Ikeda and then further in combination with the Sakamoto reference. Claims 5 and 6 are directed to the elements making up the double sampling circuit which includes an AC couple device, as well as a CMOS switch and a unit gain operational amplifier. The AC couple device is connected between the integrator circuit and the unit gain operational amplifier and the CMOS switch is connected between a reference voltage source and a transmission path of the AC couple device and the unit gain operational amplifier. However, both Claims 5 and 6 are ultimately dependent upon now amended Independent Claim 1 and are believed to show patentable distinctions for the reasons as previously discussed with regard to the Mizuno reference, the Ikeda reference, and the Sakamoto reference, in the discussion of patentability of Claim 1 as amended.

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It is respectfully submitted that the combination of features now recited in the amended Claims of the subject Patent Application are nowhere shown nor suggested in the reference cited by the Examiner. Thus, it is believed that Applicant's invention, as now claimed, is neither anticipated nor made obvious by that reference.

It is believed that the Dependent Claims add further patentably distinct limitations, but are at least patentably distinct for the same reasons as Independent Claim 1 upon which they are dependent, and therefore should be allowed.

It is now believed that the subject Patent Application has been placed fully in condition for allowance, and such action is respectfully requested.

The Director is hereby authorized to pay any deficiencies in fees associated with the filing of this Reply, should there be any, from Deposit Account # 18-2011.

Respectfully submitted,

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